EE / CPRE / SE 491 - sdmay20-38
iFPGA - Intermittent Intelligent FPGA Platform
Week7 Report

2/12/20 - 2/26/20
Client: Henry Duwe
Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus
Jake Meiss - Team member, HW focus
Andrew Vogler - Team member, FPGA focus
Zixuan Guo - Team member, FPGA focus
Justin Sung - Team member, FPGA focus

Weekly Summary

- Continue working on the SPI connection implementation.
- Continued work on schematics for PCB design
- Confirm functionality and accuracy of the Librosa library and other open-source libraries for sound processing
- Port the MAC design into Libero IDE and confirm functionality

Past Week Accomplishments

- MAC Design - Zixuan Guo
    - Completed the MAC implementation
    - Designed an AMBA data bus protocol to be used for internal communications on the FPGA

- PCB Design - Jake Meiss
    - Continued work on schematics including data signals, control of flash freeze mode, creation of symbols for oscillators, adding decoupling capacitors, etc.
    - Updated parts list with current discrete component selections

- SW - Jake Tener
    - Creation of testing programs that will analyze .wav files
    - Explored the Aquila libraries and generated an MFCC to be compared against Librosa generation.
    - Evaluated differences in sound analysis between Aquila and Librosa, then evaluated differences in MFCC calculation
    - Recreate the Neural Network for Aquila library in C++, not Liberosa

- HW - Justin Sung, Andrew Vogler

    - Continued progress towards establishing SPI data communications between the MSP430 and the NANO.

Pending Issues

- The SPI connection is taking longer than we expected due to poor documentation. We brought this up with Duwe and He understands the situation we are in for this aspect of the project.
- C library being used may not work as we think. That may or may not be a problem. TBD. Explore other C/C++ libraries able to handle MFCC generation
- Consider Retraining the neural network for Aquila, not Liberosa

Individual Contributions

Team Member	**Contribution**	**Weekly Hours**	**Total Hours**
Jake Tener	SW	13	41
Jake Meiss	PCB Design	20	48
Andrew Vogler	HW	14	42
Zixuan Guo	MAC Design	13	41
Justin Sung	HW	15	43

Plans for Coming Week

- Establish SPI communications
    - Be able to write data from MSP430 to NANO memory
    - Be able to write data from NANO to MSP430
- Integrate the MAC design into Libero IDE
- Electrical Design
    - Finish the preliminary schematics and begin to get them checked
    - Start on the layout for the PCB
- Software
    - Finish C program that will generate MFCC coefficients for a .wav file